REMARKS

Applicants respectfully traverse and request reconsideration.

Examiner Conference

Applicants wish to thank the Examiner for the courtesies extended to Applicants' attorneys, Christopher J. Reckamp (Reg. No. 34,414) and William J. Voller III, acting on behalf of and under the supervision of Christopher J. Reckamp, (collectively, "Applicants' Attorneys) during telephonic conferences held between Applicants' Attorneys and Examiner Lillian Vo ("Examiner") on November 15, 2007. During a conference with William J. Voller III ("Voller"), Voller and Examiner generally discussed the networked computer configuration taught in the cited portions of U.S. Patent No. 6,098,091 to Kisor ("Kisor") in view of proposed claim language directed to, among other things, processing resources in a homogenous multiprocessor environment in an integrated circuit where the available processors in the integrated circuit are operatively coupled to a bus in the integrated circuit. The Examiner preliminarily agreed that the cited portions of Kisor, alone or in combination with the other references, did not appear to teach or suggest this proposed language.

Claim Amendments

Claims 15 and 19 have been cancelled without prejudice. Claims 22-23 are new. Claims 5, 7-11 and 16-18 and 20 have been amended. Applicants believe that no new matter has been added in the aforementioned claim amendment. For example, the subject matter presented in amended claims 16-18 have support at least on page 4 and in FIG. 3 of the originally-filed application.

Objections

Citing 35 U.S.C. § 101, the Office action states that if claim 15 should be found allowable, claim 18 will be objected to under 37 CFR § 1.75 as being a substantial duplicate thereof. Preliminarily, Applicants note that claims 15 and 18, as previously presented, had different scopes for at least the reason that claim 15 was directed to a method that, among other things, "provid[es] to the available processing resources functional programs and initial data corresponding to the tasks", whereas claim 18 was directed to a method that, among other things, "provid[es] to the available processing resources functional programs corresponding to the tasks." (Emphasis noted). Irrespective of this distinction, the potential objection is moot in view of the cancellation of claim 15.

Claim Rejections

Claims 2-12, 15-16 and 18 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,098,091 to Kisor ("Kisor") in view of U.S. Patent No. 5,706,514 to Bonola ("Bonola"). Claim 17 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Bonola in view of Kisor. Claims 19-21 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Kisor in view of Bonola as applied to claims 15, 16 and 18 above, and further in view of U.S. Patent No. 6,338,130 to Sinibaldi et al. ("Sinibaldi").

Independent Claims

Claims 15-18

Claim 15 has been cancelled. Claims 16-18 each contain limitations generally directed to a homogeneous multiprocessor environment in an integrated circuit or a plurality of homogeneous processors in an integrated circuit, wherein the processors in the integrated circuit are operatively coupled to a bus. Each of claims 16-18 also contain limitations that generally

require the identification of available processing resources independent of the tasks (e.g., claims 16 and 18) or that require the dynamic allocation of tasks to available processing resources without regard to a processor mode (e.g., claim 17).

Kisor is directed to a method and system that includes a central computer that assigns tasks to idle workstations using availability schedules and computational capabilities. (Title). Kisor expressly states that the method and system assigns tasks to peer-to-peer computers connected via a wide area network. (Abstract, Emphasis added). As used by Kisor, peer-to-peer computers appear to be independent systems, and not a homogenous multiprocessor environment in an integrated circuit. For example, Kisor states that examples of peer-to-peer computers are computers or workstations as manufactured by IBM, Apple and Sun. Kisor states that "[e]ach computer may be coupled to other computers in the Internet network via a variety of communication techniques." (Col. 3, ll. 18-43; Fig. 1, Emphasis added). Applicants submit that, unlike a homogeneous multiprocessor environment (or a plurality of homogeneous processors) in an integrated circuit wherein each of the available processors in the integrated circuit is operatively coupled to a bus in the integrated circuit, peer-to-peer computers coupled over an Internet network, like in Kisor, require different and more complex protocols for communication. Accordingly, Kisor does not appear to contemplate Applicants' claimed subject matter that includes a homogeneous multiprocessor environment (or a plurality of homogeneous processors) in an integrated circuit where each processor in the integrated circuit is operatively coupled to a bus.

As characterized by Applicants in previous papers with the Office, Bonola is directed to the distributed execution of mode mismatched commands in multiprocessor computer systems. Accordingly, Bonola teaches that a CPU processes a command if the operating mode of the CPU

matches the mode of the current command. If the CPU and command are not mode-matched, then slave CPUs are polled to determine if one of the slave CPUs are in a mode that matches the current command. If there is a match, then a slave CPU processes the command. Alternatively, Bonola relies on emulation to process the mode mismatched command. (Col. 1; Col. 2, ll. 19-28; Col. 2, l. 53 – Col. 3, l. 2; Col. 3, ll. 5-30, Col. 7, ll. 35-50). Accordingly, Bonola does not teach or suggest each limitation of claims 16-17 because processing of a command is always based on a task or the mode.

Further, the combination of Kisor and Bonola does not teach or suggest the claimed subject matter because no combination of these publications teaches or suggests the claimed identification of available processing resources in the homogeneous multiprocessor environment independent of the tasks, wherein each of the available processors in the integrated circuit is operatively coupled to a bus in the integrated circuit as in claims 16 and 18. Nor does any combination of Kisor and Bonola teach or suggest a plurality of homogeneous processors in an integrated circuit coupled to a bus in the integrated circuit, wherein the claimed kernel program code is configured to dynamically allocate the processing of the program code among the plurality of processors without regard to a processor mode, as in claim 17. Instead, any combination of Kisor and Bonola necessarily consists of Kisor's peer-to-peer computers networked over the Internet in contrast to Applicants' claimed homogeneous multiprocessor environment (or plurality of processors in an integrated circuit) where each processor is operatively coupled to a bus in the integrated circuit. Any combination of Kisor and Bonola would also yield a system capable of handling the distributed execution of mode mismatched commands and not be capable of identifying available processing resources in the homogeneous multiprocessor environment independent of the tasks or be capable of dynamically allocating the

processing of the program code among the plurality of processors without regard to a processor mode.

Because the aforementioned limitations would not be taught by any combination of Kisor and Bonola, Applicants respectfully submit that each of claims 16-18 are in proper condition for allowance.

New Claim 23

Claim 23 requires, among other things, a plurality of homogeneous processors coupled to a bus in the apparatus and kernel program code configured to dynamically allocate the processing of the program code among the plurality of processors without regard to a processor mode.. Applicants submit that no combination of prior art references teaches or suggests the claimed subject matter of new claim 23. In addition to reasserting the relevant remarks made above with respect to claims 16-18, Applicants respectfully submit that Kisor appears to be directed to peer-to-peer computers connected via a wide area network such as an Internet network and thus is not directed to a plurality of homogeneous processors coupled to a bus in the apparatus. Applicants further note that Kisor appears to require different and more complex protocols for communication between the peer-to-peer computers than would be required for an apparatus comprising a plurality of homogeneous processors coupled to a bus in the apparatus. For example, Applicants submit that Kisor may require http-compliant protocols and/or multiple sessions to initialize communication over the network. For at least each of these reasons, claim 23 is believed to be in proper condition for allowance.

Dependent Claims

Claims 2-12, 21 and 22 depend on allowable claim 18. Claim 20 depends on allowable claim 16. For at least the reasons presented above, the aforementioned dependent claims are also

believed to include additional patentable, novel and non-obvious subject matter. For example, claims 20 and 21 require that the allocation of available processing resources among the tasks based on the capabilities of each of the available processors of the homogeneous multiprocessor environment comprises allocating the available processing resources among the tasks based on the ability of each of the available processors of the homogeneous multiprocessor environment to be aggregated with another processors of the homogeneous multiprocessor environment to provide a processing resource. The subject matter presented in claims 20 and 21 appears to stand rejected in view of Kisor as modified by Bonola: Col. 7, ll. 36-38, 42-52, 57-61; Col. 8, ll. 11-18, 46-65; Col. 9, ll. 12-23; and Sinibaldi: Col. 12, l. 59 – Col. 13, l. 5; Col. 13, ll. 28-46; Col. 19, ll. 40-52. Applicants submit that no combination of Kisor, Bonola and Sinibaldi teaches or suggests the claimed subject matter presented above.

As to the cited portions of Bonola, Applicants submit that the cited portions of Bonola rely on a slave_available software or watchdog timer to determine the amount of time that a host CPU should wait to determine if a slave CPU is available for processing a mode-mismatched command before the host falls back to conventional processing of the mode-mismatched command using emulation. (Col. 7, ll. 25-30). If a slave CPU is available before the timer expires, control passes to it and memory is made available to the slave CPU for the processing of the mode-mismatched command. (Col. 8, ll. 11-18). Thereafter, the slave CPU is reset prior to processing the mode-mismatched command. (Col. 8, ll. 46-67; Fig. 3B, steps 1050). The mode-mismatched command is processed by the recently-reset slave CPU (Fig. 3B, step 1060) and when finished, the results are obtained from a common memory block (Fig. 3B, step 1070). (Col. 9, ll. 1-24). In other words, Bonola teaches a processor by which a host CPU waits a predetermined amount of time to determine if a slave CPU is available to process a mode-

mismatched command. If a slave CPU is available, it processes the mode-mismatched command after being reset. If a slave CPU is not available, the host CPU processes the mode-mismatched command using emulation. Applicants are unable to find any relationship between these cited portions of Bonola and the identified subject matter of claims 20 and 21, wherein the allocation of available processing resources is based on the ability of each of the available processors of the homogeneous multiprocessor environment to be aggregated with another processor of the homogeneous multiprocessor environment to provide a processing resource.

Sinibaldi is directed to an adaptive method an apparatus for allocation of DSP resources in a communication system that includes at least one DSP and a WAN driver. (Title, Abstract). The WAN driver receives task allocation requests from a host to open or close communication channels that are handled by the at least one DSP. Each task is allocated to one of the at least DSP according to a total current task processing load for each of the at least one DSP, a maximum processing capability for each of the at least one DSP, and a processing requirement for each task being allocation to the one of the at least one DSP that can handle the additional processing load of the task being allocated. (Abstract).

The cited portions of Sinibaldi generally relate to the open channel communication process illustrated in FIG. 15. In this process, Sinibaldi appears to teach that the WAN driver operates to handle load leveling of new tasks and to distribute new tasks over the at least one DSP in the adapter card to make best use of the available processing capability of each of the at least one DSP in the adapter card. (Col. 13, ll. 1-10; Fig. 15, step 1504). When a new task is received, a new channel is opened and a look-up table is used to identify the number of MIPs of the task. (Col. 13, ll. 6-10). The WAN driver then accumulates the total current MIPS being handled for all current tasks by each of the at least one DSP to determine a current MIP

processing total being handled by each of the at least one DSP and then appears to attempt to select a single DSP that can handle the new task MIP requirements. (Col. 13, ll. 10-36; Fig. 15, steps 1510-1512). The selected, single DSP performs the task and as tasks are completed, channels are closed and the load tables are updated. (Col. 13, ll. 37-46).

At best, Sinibaldi compares available resources in a multiple DSP environment to assign a task having an established MIP requirement to a single, available DSP. Applicants are unable to find any teaching or suggestion in Sinibaldi, alone or in combination with Bonola and Kisor, in which available processing resources are allocated among the tasks based on the capabilities of each of the available processors of the homogeneous multiprocessor environment and further based on the ability of each of the available processors of the homogeneous multiprocessor environment to be aggregated with another processor of the homogeneous multiprocessor environment to provide a processing resource. In fact, it appears that DSPs in Sinibaldi are unable to be aggregated to provide a processing resource as the process described above appears to assign the processing of a new task to a single DSP.

Accordingly, Applicants respectfully submit that the claims are in condition for allowance and that a timely Notice of Allowance be issued in this case. The Examiner is invited to contact the below-listed attorney if the Examiner believes that a telephone conference will advance the prosecution of this application.

Respectfully submitted,

Date: November 19, 2007

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